REMARKS

This Amendment is filed in response to the Office Action mailed June 8, 2006. All objections and rejections are respectfully traversed.

Claims 1-15 and 18 are pending in the case.

Claims 16 and 17 have been cancelled without prejudice.

Claims 1, 5, 6, 9, 10-12, 14 and 15 have been amended.

Claim 18 has been added.

The specification has been minorly amended. No new matter has been introduced.

Claim Rejections - 35 U.S.C. §101

At page 2 of the Office Action, claim 17 was rejected under 35 U.S.C. §101 as directed to non-statutory subject matter. The Applicant has cancelled claim 17, and accordingly this rejection is believed to be moot.

Claim Rejections - 35 U.S.C. §102

At pages 2-3 of the Office Action, claims 1-15[1] were rejected under 35 U.S.C. §102(b) as anticipated by Peterson et al., U.S. Patent No. 5,168,499 (hereinafter Peterson).

The Applicant's claim 1, representative in part of the other rejected claims, sets forth:

> 1. Apparatus for enhancing debug capability in a multiprocessor circuit, comprising:
>
> a plurality of processors arranged so that data advances from processor to processor during normal operation, each processor being a part of a processor complex that includes a first context memory for data to be processed, and a second

[1] While the top of page 3 of the Office Action states claim 16 is also rejected under 35 U.S.C. §102(b), the Applicant assumes this is a typographical error given that no further discussion of claim 16 is found in this section of the Office Action, and claim 16 is later rejected under 35 U.S.C. §103. If it is not, the Applicant respectfully requests clarification.

context memory for data that has been processed;

an advancement circuit, the advancement circuit configured to advance data among the processors in the event of failure of a processor; and

a data bypass circuit configured to pass the data through the processor complex with the failed one of the processors, by moving the data from the first context memory to the second context memory of that processor complex absent processing.

Peterson discloses a fault detection and bypass circuit for use with a systolic array of processors. If an error is detected, a signal is sent to a multiplexer located between the failed processor element and the subsequent processor element of the array. *See* col. 7, lines 15-20. The multiplexer is configured to receive two inputs, one connected to the output data path of the failed processor element, and one connected to the input data path of the failed processor element. *See* col. 15, lines 59-64 and Fig. 19. When triggered, the multiplexer directs data around the failed processor element, so that data does not pass therethrough. *See* col. 15, line 65 to col. 16, lines 6 and Fig. 19.

The Applicant respectfully urges that Peterson is silent concerning the Applicant's claimed "***a data bypass circuit configured to pass the data through the processor complex with the failed one of the processors, by moving the data from the first context memory to the second context memory of that processor complex absent processing***."

While the Applicant claims moving data ***<u>through</u> the processor complex with the failed one of the processors … absent processing,*** Peterson in contrast discloses using a multiplexer and dedicated bypass pathways (shown in Peterson's Fig. 19, but unlabeled) to completely bypass a failed processing element and its related circuitry. Peterson's dedicated bypass pathways add additional traces and complexity to the systolic array design. The Applicant recognizes, as discussed in the specification at page 18, lines 22-27 that manufacturing defects are mostly associated with certain parts of processing complexes and that some portions rarely contain defects. For example, context memories "are not as susceptible to defects and may in fact be operational even after other elements of the PE are defective." Thus, rather than use additional dedicated pathways to bypass a processing complex with a failed processor, the Applicant claims passing data ***<u>through</u> the***

processor complex, in part using the context memories that are already there. Patterson in no way suggests this feature.

Accordingly, the Applicant respectfully urges that Peterson is legally insufficient to anticipate the present claims under 35 U.S.C. §102(b) because of the absence of the Applicant's claimed novel "***a data bypass circuit configured to pass the data through the processor complex with the failed one of the processors, by moving the data from the first context memory to the second context memory of that processor complex absent processing***."

Claim Rejections - 35 U.S.C. §103

At pages 5-6 of the Office Action, claim 16 was rejected under 35 U.S.C. §103(a) as anticipated by Peterson et al., U.S. Patent No. 5,168,499 (hereinafter Peterson) in view of Tanenbaum, *Structure Computer Organization,* Third Edition.

Claim 16 is no longer pending in the case.

In the event that the Examiner deems personal contact desirable in disposition of this case, the Examiner is encouraged to call the undersigned attorney at (617) 951-2500.

In summary, all the independent claims are believed to be in condition for allowance and therefore all dependent claims that depend there from are believed to be in condition for allowance. The Applicant respectfully solicits favorable action.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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